Synopsis V1.0
Proton SEE Test of Gflx Process SRAM Test Vehicle from LSI Logic

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I. Introduction

This study was undertaken to determine the proton induced single event destructive and transient susceptibility of the LSI Logic Gflx standard process and two versions of Gflx radiation hardened process. The test vehicle is a SRAM. The device under test (DUT) was monitored for single event upset (SEU) and for destructive events induced by exposing it to a proton beam at the Indiana University Cyclotron Single Event Effects Test Facility.

II. Devices Tested

LSI Logic Gflx standard technology is a 0.11 μm CMOS bulk process. The two versions of the radiation-hardened process include a buried layer in order to guarantee SEL immunity.

The SRAM test vehicle L9B0422 (RAM187 high density module and RAM249 high speed module) is a 4Mbit SRAM organized as 512K*8 bits externally. The test vehicle uses internally 16 256Kbit memory megacells. The core SRAM cell is a 6-transistor cell. The memory core supply voltage is 1.2V, and the I/O supply voltage is 2.5V. The SRAM test vehicle is packaged in a 64 pin plastic quad flat pack (PQFP) (code UC36).

The test samples' package markings are shown in tables 1 and 2.

Table 1: RAM249 test samples

Test vehicle	Process	Marking	SN#
RAM249	Standard (ctrl)	LSI Logic L9B0421 GAH15900.14 ETH27001.1 Control B2 24 G 0528 Δ Korea	2
	Buried layer 1 (Dose 5)	LSI Logic L9B0421 GAH15900.14 ETH27001.1 1.6M5E14B2 12 G 0528 Δ Korea	19
	Buried layer 2 (Dose 1)	LSI Logic L9B0421 GAH15900.14 ETH27001.1 1.6M1E14B2 7 G 0528 Δ Korea	32, 36

Table 2: RAM187 test samples

Test vehicle	Process	Marking	SN#
RAM187	Standard (ctrl)	LSI Logic L9B0421 GAH15900.14 ETH27002.1 Control BR 24 G 0528 Δ Korea	51
	Buried layer 1 (Dose 5)	LSI Logic L9B0421 GAH15900.14 ETH27002.1 1.6M5E14BR 12 G 0528 Δ Korea	66
	Buried layer 2 (Dose 1)	LSI Logic L9B0421 GAH15900.14 ETH27002.1 1.6M1E14BR 7 G 0528 Δ Korea	82

III. Test Facility

Facility: Indiana University Cyclotron Facility (IUCF), Bloomington, IN

Energy: 200 MeV, 104 MeV
Flux: 1 x 10^7 to 1 x 10^8 particles/cm^2/s depending on device sensitivity.
Fluence: All tests will be run to 1 x 10^{10} p/cm^2 or until destructive at least 100 SEU occurred.

IV. Test Conditions and Error Modes

Test Temperature: Room Temperature
Operating Frequency: static, dynamic 10 MHz
Power Supply Voltage: memory core: 1.2V, I/Os: 2.5V

PARAMETERS OF INTEREST: Power supply currents, device functionality

SEE Conditions: SEL, SEU, MEU, SET

V. Test Methods

Both test vehicles were tested with NASA-GSFC REAG (Radiation Effects and Analysis Group) Low Cost Digital Tester (LCDT). LCDT is a reusable universal digital device tester based on Xilinx Spartan 3 Field Programmable Gate Array (FPGA) with input/output (I/O) operation speed up to 200 MHz.
LCDT is the main test board that interfaces with the DUT-specific daughter card. The DUT on the daughter card is exercised using the configurable FPGA on LCDT with Hardware Design Language such as VHDL based coding. A remote PC controls LCDT. Figure 1 shows the LCDT with the SRAM daughter board.

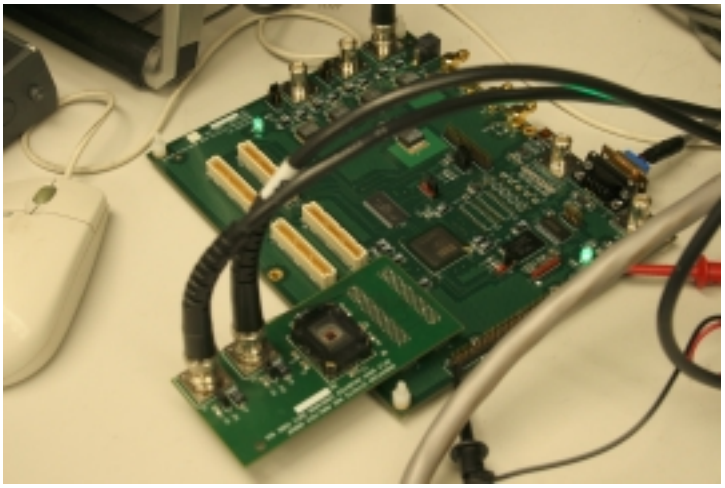

Figure 1: LCDT with SRAM daughter board

During irradiation, DUT power supply currents (core and I/Os) were monitored. As soon as on of the current reaches a programmable (20 mA for the core, 10 mA for I/Os) SEL detection level, the DUT power supplies were shutdown.

SRAM test vehicle was tested under two different test conditions:

- static test: a test pattern is loaded in the DUT before irradiation. DUT is irradiated. Then, it is checked after the end of the irradiation run.
- Dynamic test: a test pattern is loaded in the DUT before irradiation. During irradiation DUT is continuously read and errors are corrected in real time. Error information (address, data read, expected data) is stored for further analysis (MEU, stuck bits,..). Figure 2 below shows the dynamic test flow diagram.

Four different test patterns were used: all0, all1, logical checkerboard, and reverse logical checkerboard.

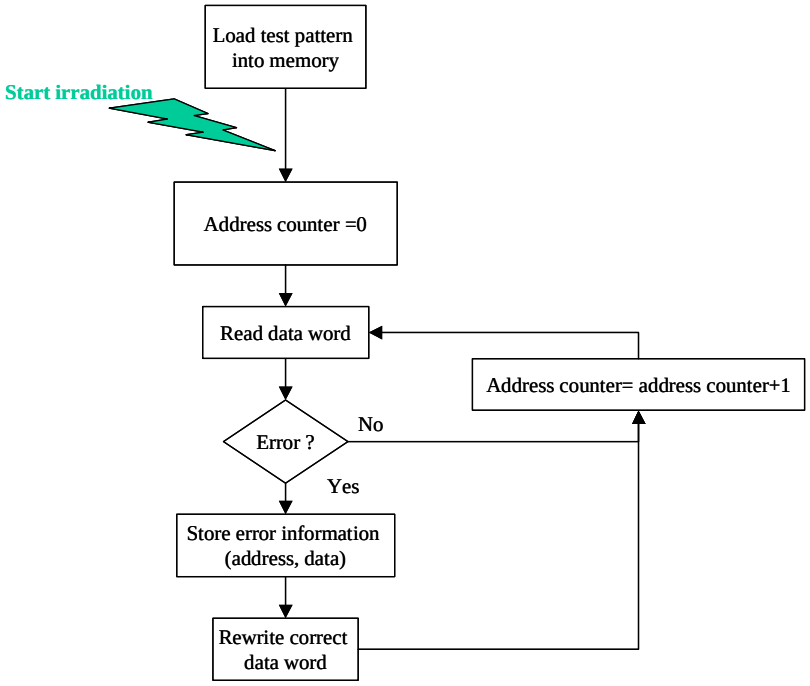

Figure 2: dynamic test flow diagram

VI. Test results

Detailed test results are given in Appendix. Test data showed little part-to-part variation, no test condition effect, static versus dynamic, and little effect on test pattern. Results presented below are average results between test samples and test patterns. No micro lachup event was observed during proton tests. Protons SEU cross sections are shown in Figure 3. We can see that both RAM designs have a similar SEU sensitivity. The maximum measured cross section is about 2 10^{-14} cm^2/bit.

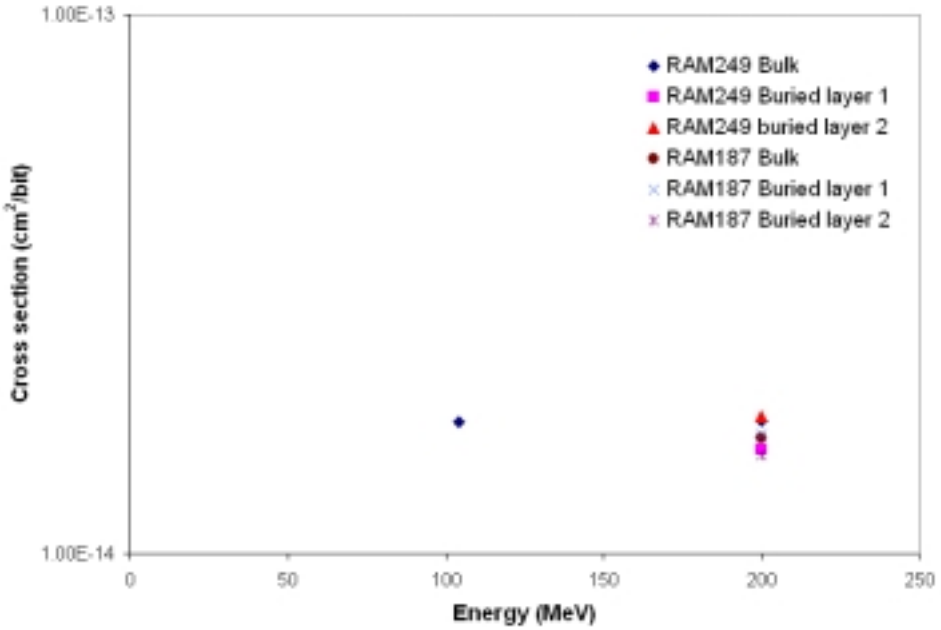

Figure 3: proton SEU cross-section curve

Reference documents:

- "Gflx SRAM Test Chip Design MEMPQV," file MEMPQV_spec.pdf, Nov 1, 2001.
- "Low cost digital tester hardware manual," 2005.

Appendix: Test Results

Run #	Process	SN	Test mode	Pattern	Energy (MeV)	Fluence (#/cm^2)	SEU #	Xsec (cm^2/dev)	Comment
6	249 bulk	2	dynamic	all1	200	5.00E+09	347	6.94E-08	
7	249 bulk	2	static	all1	200	1.25E+09	111	8.88E-08	
8	249 bulk	2	dynamic	all0	200	5.00E+09	318	6.36E-08	
9	249 bulk	2	static	all0	200	5.00E+09	311	6.22E-08	
10	249 bulk	2	dynamic	aaaa	200	3.12E+09	201	6.44E-08	
13	249 bulk	2	static	aaaa	200	5.00E+09	383	7.66E-08	
14	249 bulk	2	dynamic	all1	200	5.00E+09	393	7.86E-08	
15	249 bulk	2	static	all1	200	5.00E+09	365	7.30E-08	
16	249 bulk	2	dynamic	all0	200	5.00E+09	418	8.36E-08	
17	249 bulk	2	static	all0	200	5.00E+09	403	8.06E-08	
18	249 bulk	2	dynamic	all1	200	5.00E+09	325	6.50E-08	80 deg incidence
19	249 bulk	2	static	all1	200	5.00E+09	333	6.66E-08	80 deg incidence
20	249 bulk	2	dynamic	all0	200	5.00E+09	375	7.50E-08	80 deg incidence
21	249 bulk	2	static	all0	200	5.00E+09	364	7.28E-08	80 deg incidence
22	249 BL2	32	dynamic	all1	200	5.00E+09	332	6.64E-08	
23	249 BL2	32	static	all1	200	5.00E+09	382	7.64E-08	
26	249 BL1	19	dynamic	all0	200	5.00E+09	322	6.44E-08	
27	249 BL1	19	dynamic	all1	200	5.00E+09	314	6.28E-08	
28	249 BL1	19	static	all1	200	5.00E+09	344	6.88E-08	
29	249 BL1	19	static	all0	200	5.00E+09	332	6.64E-08	
30	249 BL2	36	dynamic	all1	200	5.00E+09	330	6.60E-08	
31	249 BL2	36	dynamic	all0	200	5.00E+09	410	8.20E-08	
32	249 BL2	36	static	all1	200	5.00E+09	416	8.32E-08	
33	249 BL2	36	static	all0	200	5.00E+09	390	7.80E-08	
34	187 bulk	51	dynamic	all1	200	5.00E+09	323	6.46E-08	
36	187 bulk	51	dynamic	all0	200	5.00E+09	343	6.86E-08	
37	187 bulk	51	static	all1	200	5.00E+09	369	7.38E-08	
38	187 bulk	51	static	all0	200	5.00E+09	337	6.74E-08	
39	187 BL2	82	dynamic	all1	200	5.00E+09	325	6.50E-08	
40	187 BL2	82	dynamic	all0	200	5.00E+09	309	6.18E-08	
41	187 BL2	82	static	all1	200	5.00E+09	308	6.16E-08	
43	187 BL2	82	static	all0	200	5.00E+09	333	6.66E-08	
44	187 BL1	66	dynamic	all1	200	5.00E+09	347	6.94E-08	
45	187 BL1	66	dynamic	all0	200	5.00E+09	354	7.08E-08	
46	187 BL1	66	static	all1	200	5.00E+09	331	6.62E-08	
47	187 BL1	66	static	all0	200	5.00E+09	360	7.20E-08	
48	249 bulk	2	dynamic	all1	104.2	4.81E+09	308	6.40E-08	
49	249 bulk	2	dynamic	all0	104.2	5.00E+09	334	6.68E-08	
50	249 bulk	2	static	all1	104.2	5.00E+09	402	8.04E-08	
52	249 bulk	2	static	all0	104.2	1.09E+09	91	8.33E-08	